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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/052,244	01/23/2002	Katsuhito Sasaki	OKI.295	5830

7590 04/07/2003

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EXAMINER	
GARCIA, JOANNIE A	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 04/07/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/052,244	SASAKI, KATSUHITO	
	Examiner	Art Unit	
	Joannie A García	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 January 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 1-18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, lines 6 and 12, "a" before "gate oxide layer" should be replaced with --of said--.

In claim 1, line 11, --step-- should be preceded by "implanting ions".

In claim 7, lines 8 and 15, "a" before "gate oxide layer" should be replaced with --of said--.

In claim 7, line 14, --step-- should be preceded by "implanting ions".

In claim 13, lines 8 and 17, "a" before "gate oxide layer" should be replaced with --of said--.

In claim 13, line 16, --step-- should be preceded by "implanting ions".

Claims 1, 5-7, 11-13, 17, and 18, are rejected under 35 U.S.C. 102(a) as being anticipated by Efland et al.

The rejection is maintained as stated in the Office Action mailed 12-19-02, and as stated below.

Efland et al discloses manufacturing an LDMOS transistor comprising providing a semiconductor substrate 11of a first conductivity type having a well region 32 of a second

conductivity type formed on a surface thereof (Figure 3, Column 4, lines 7-8, and 13-14), implanting ions of the first conductivity type into a part of the well region (Column 3, lines 26-27), forming a gate oxide layer 39 on the surface of the semiconductor substrate (Figure 3, Column 3, lines 23-24, and Column 4, lines 13-18), said forming of said gate oxide layer including subjecting the semiconductor substrate to a heat treatment (Column 3, lines 23-24 and Column 4, lines 13-18), diffusing the implanted ions to form a diffusion region 33 of the first conductivity type on the surface of the semiconductor substrate (Figure 3, Column 3, lines 26-27, and Column 4, line 14), forming a gate electrode 38 on the surface of the semiconductor substrate (Figure 3, and Column 4, lines 14-16), and forming a reduced surface drain 31 on the surface of the semiconductor substrate within the first region (Figure 3, and Column 4, lines 19-20), wherein said implanting ions step could be carried out with an energy set so that an accelerated oxidation during formation of the gate oxide layer is inhibited to achieve formation of diffusion region 33 (Figure 3), and wherein said implantation is conducted into a region of the semiconductor substrate where the drain region is formed (Figure 3).

Efland et al discloses as well, manufacturing an LDMOS transistor comprising providing a semiconductor substrate 11of a first conductivity type having a first well 32 of a second conductivity type formed on a surface thereof within a first region (Figure 3, Column 4, lines 7-8, and 13-14), and a second well 33 of the first conductivity type formed within a second region that is inside of the first region (Figure 3, Column 4, lines 7-8, and 14), implanting ions of the second conductivity type into the second well (Column 3, lines 26-27), forming a gate oxide layer 39 on the surface of the semiconductor substrate, the gate oxide layer extending from the first region to the third region through the second region (Figure 3, and Column 4, lines 15-18),

said forming of said gate oxide layer including subjecting the semiconductor substrate to a heat treatment (Column 3, lines 23-24 and Column 4, lines 13-18), diffusing the implanted ions to form diffusion region 34 of the second conductivity type located in a third region that is inside of the second region (Figure 3, Column 3, lines 26-27, and Column 4, line 14), forming a gate electrode 38 on the surface of the semiconductor substrate, the gate oxide layer extending from the first region to the third region through the second region (Figure 3, and Column 4, lines 15-18), and forming a reduced surface drain 31 on the surface of the semiconductor substrate within the first region (Figure 3, and Column 4, lines 19-20), wherein said implanting ions could be carried out with an energy set so that an accelerated oxidation during formation of the gate oxide layer is inhibited to achieve formation of diffusion region 34 (Figure 3), and wherein said implantation is conducted into a region of the semiconductor substrate where the drain region is formed (Figure 3).

Applicant argues that Efland et al does not remotely suggest implanting ions into a well region, and subsequently forming a gate oxide thereon, wherein the gate oxide formation includes subjecting the substrate to a heat treatment to diffuse the implanted ions. However, Efland et al discloses formation of diffused regions by implantation (Column 1, lines 17-19, Column 3, lines 18-21, and 26-27), and growing a gate oxide thereon, therefore, subjecting the substrate to a heat treatment, diffusing implanted ions. Furthermore, Efland et al incorporates therein reference U.S. patent Ser. No. 60/047,474, entitled "Reduced Surface Drain (RSD) LDMOS Power Device", to Tsai et al (Column 4, lines 8-13), wherein implantation and diffusion of various materials is recited (Page 8, lines 9-12), and more specifically, formation of diffused region 13 by implantation (Figure 3, and Page 10, liens 1-3).

Applicant argues that Efland et al does not remotely suggest implanting ions, prior to gate oxide formation, so that an accelerated oxidation during subsequent formation of a gate oxide layer is inhibited. However, the ion implantation is set to be carried out with an energy so that an accelerated oxidation during formation of the gate oxide layer is inhibited, achieving formation of Efland's et al diffusion regions (Figure 3, and Column 4, lines 13-15). One of ordinary skill in the art would have been led to the recited implant energy through routine experimentation within the teachings of Efland et al to achieve desired device dimensions and desired device characteristics on the finished wafer. Further, the oxidation is necessarily inhibited with respect to a process that employs higher energy and/or dose.

Claims 2-4, 8-10, and 14-16, are rejected under 35 U.S.C. 103(a) as being unpatentable over Efland et al as applied to claims 1, 5-7, 11-13, 17, and 18 above, and further in view of the following comments.

The rejection is maintained as stated in the Office Action mailed 12-19-02, and as stated above.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group Receptionist whose telephone number is (703) 308-0956. **See MPEP 203.08**.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner J. Garcia whose telephone number is (703) 306-5733. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (703) 306-2794. The fax number for this group is (703) 308-7722 (and 7724), and (703) 305-3431 (and 3432). MPEP 502.01 contains instructions regarding procedures used in submitting responses by facsimile transmission.

JAG
4/4/03

George Fourson
Primary Examiner